Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An interface circuit conforming to multiple bus standards, comprising:

a first interface circuit conforming to a first bus standard;

a second interface circuit conforming to a second bus standard; and

a common set of pins coupled to the first interface circuit and the second interface circuit and a host computer bus, the common set of pins being user selectable to communicate with [[a]] the host computer bus in accordance with either the first bus standard or the second bus standard.

Claim 2 (currently amended): The interface circuit of claim 1, wherein the common set of pins is configured to transmit and receive data conforming to either ~~the~~ a PCI bus standard or ~~the~~ a PCMCIA bus standard.

Claim 3 (currently amended): The interface circuit of claim 1, wherein the first bus standard [[is]] comprises a PCI standard.

Claim 4 (currently amended): The interface circuit of claim [[1]] 3, wherein the second bus standard [[is]] comprises a PCMCIA standard.

Claim 5 (original): The interface circuit of claim 1, further comprising a multi-voltage input output buffer coupled to each pin.

Claim 6 (original): The interface circuit of claim 1, further comprising an internal bus coupled to the first and second interface circuit.

Claim 7 (currently amended): The interface circuit of claim 6, wherein the first interface circuit is configured to format ~~formats~~ signals on the internal bus to signals compliant with the first bus standard.

Claim 8 (currently amended): The interface circuit of claim [[1]] 7, wherein the second interface circuit is configured to format ~~formats~~ signals on the internal bus to signals compliant with the second bus standard.

Claim 9 (original): The interface circuit of claim 1, further comprising a first power supply to supply voltage swings in accordance with the first bus standard.

Claim 10 (currently amended): The interface circuit of claim [[1]] 9, further comprising a second power supply to supply voltage swings in accordance with the second bus standard.

Claim 11 (new): A peripheral device comprising:

a peripheral circuit;

a first signal translator coupled to the peripheral circuit via a first bus, the first signal translator configured to format signals from the first bus to a first protocol;

a second signal translator coupled to the peripheral circuit via the first bus, the second signal translator configured to format signals from the first bus to a second protocol; and

a buffer circuit coupled to the first signal translator and the second signal translator, the buffer circuit to communicate the signals of either the first protocol or the second protocol to a system to which the peripheral device is coupled.

Claim 12 (new): The peripheral device of claim 11, wherein the buffer circuit comprises a multi-voltage buffer.

Claim 13 (new): The peripheral device of claim 12, wherein the multi-voltage buffer comprises a buffer having a voltage input coupled to a switch controllable to couple to a first voltage or a second voltage.

Claim 14 (new): The peripheral device of claim 11, wherein the buffer circuit is to receive incoming signals from the system at a voltage higher than a supply voltage of the peripheral device.

Claim 15 (new): The peripheral device of claim 11, wherein the peripheral circuit comprises a wireless device configured to communicate via different protocols over a cellular medium and a short-range radio medium.

Claim 16 (new): The peripheral device of claim 11, wherein the peripheral device is user selectable to communicate with the system via the first protocol or the second protocol.

Claim 17 (new): A method comprising:

receiving an indication in a peripheral device of a desired mode of operation for the peripheral device; and

communicating between the peripheral device and a system coupled thereto via a first bus standard or a second bus standard based upon the indication.

Claim 18 (new): The method of claim 17, wherein receiving the indication comprises receiving a user-selectable indication in the peripheral device.

Claim 19 (new): The method of claim 17, wherein communicating between the peripheral device and the system via the first bus standard comprises communicating via a first path of the peripheral device, the first path including a common internal bus coupled between a peripheral circuit and a first bus translator, and a first bus standard bus coupled between the first bus translator and a common buffer circuit, the common buffer circuit coupled to the system.

Claim 20 (new): The method of claim 17, further comprising communicating via the first bus standard at a first set of logic levels and communicating via the second bus standard at a second set of logic levels.